an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

11. A microprocessor according to Claim 10, wherein each protection circuit is arranged to block the selection of said associated register during read and write access operations to said associated register after each resetting of the microprocessor.

12. A microprocessor according to Claim 10, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to said associated register after each resetting of the microprocessor.

13. A microprocessor according to Claim 10, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

14. A microprocessor according to Claim 10, wherein each protection circuit, during the N first operations for the selection of said associated register, compares N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

15. A microprocessor according to Claim 10, wherein a single password is provided for each register; and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison;

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

second means permitting the selection of said register if the output signal indicates that the data present on said data bus during the first operation of selection of said register corresponds to the password associated with said register.

16. A microprocessor according to Claim 15, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of said address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

17. A microprocessor according to Claim 16, wherein said second means comprises:

a delay circuit;

a two-input AND logic gate having a first input connected to the output of said address decoder for selecting the register associated with said protection circuit, a second input connected through said delay circuit to the output of said second flip-flop circuit of said first means, and an output connected to the selection input of said associated register.

18. A microprocessor according to Claim 17, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register.

19. A microprocessor comprising:

an address bus;

a data bus;

a plurality of read and write accessible registers connected to said data bus;

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register during write access operations after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

20. A microprocessor according to Claim 19, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

21. A microprocessor according to Claim 19, wherein each protection circuit, during the N first operations for the selection of said associated register, compares N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

22. A microprocessor according to Claim 19, wherein a single password is provided for each register; and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison;

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

second means permitting the selection of said register for the subsequent selection operations of said register if the output signal indicates that the data present on said data bus during the first operation of selection of the register corresponds to the password associated with said register.

23. A microprocessor according to Claim 22, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of the address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said

comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

24. A microprocessor according to Claim 23, wherein said second means comprises:

a delay circuit;

a first two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, and a second input connected through said delay circuit to the output of said second flip-flop circuit of said first means;

a second two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, and a second input receiving a read/write signal; and

an OR logic gate having a first input connected to an output of said first two-input AND logic gate, and a second input connected to an output of said second two-input AND logic gate, and an output connected to said register.

25. A microprocessor according to Claim 24, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register.

26. A microprocessor comprising:

an address bus;

a data bus;

a plurality of read and write accessible registers connected to said data bus;

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers;

each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, at least two passwords are provided to each register, and releasing of said protection circuit by a successive sending on said data bus of at least 2N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

27. A microprocessor according to Claim 26, wherein the at least two passwords for said associated register are provided over said data bus in a predetermined order.

28. A microprocessor according to Claim 26, wherein each protection circuit is arranged to block the selection of said associated register during read and write access operations to said associated register after each resetting of the microprocessor.

29. A microprocessor according to Claim 26, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to

said associated register after each resetting of the microprocessor.

30. A microprocessor according to Claim 26, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

31. A microprocessor according to Claim 26, wherein each protection circuit, during the N first operations for the selection of said associated register, compare at least 2N data elements present on said data bus with the at least 2N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register up to the next resetting of the microprocessor if the at least 2N data elements correspond to the at least 2N passwords.

32. A microprocessor according to Claim 26, wherein each protection circuit comprises:

a first protection circuit portion comprising

a first comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with a first one the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison, and

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

a second protection circuit portion connected to an output of said first protection circuit portion and comprising

a second comparator circuit for comparing, during the first operation for the selection of said register, the data element present on said data bus with a second one of the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison,

second means for holding in each protection circuit the output signal until the next resetting of the microprocessor, and

third means permitting the selection of said register for the subsequent selection operations of said register if the output signal indicates that the data present on said data bus during the first operation of selection thereof corresponds to the at least two passwords associated with said register.

33. A microprocessor according to Claim 32, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of the address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal;

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an signal output which delivers the

output signal of said comparator circuit until the next resetting of the microprocessor; and

a first delay circuit connected to the output of said second flip-flop circuit.

34. A microprocessor according to Claim 33, wherein said second means comprises third and fourth D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said third flip-flop circuit having the clock input connected to the output of said first delay circuit for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said fourth flip-flop circuit having the clock input connected to the signal output of said third flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

35. A microprocessor according to Claim 34, wherein said third means comprises:

a second delay circuit; and

a two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, a second input connected through said second delay circuit to the output of said fourth flip-flop circuit of said first means, and an output connected to the selection input of said associated register.

36. A microprocessor according to Claim 35, wherein said first and second delay circuits each comprises a shift register synchronized with the operations for the selection of said associated register.

37. A method for securing access to a plurality of registers of a microprocessor, the method comprising the steps of:

selecting one of said plurality of registers via an address decoder as a function of an address provided by an address bus connected to the address decoder;

blocking selection of the plurality of registers via a plurality of protection circuits after each resetting of the microprocessor; and

releasing a protection circuit associated with a selected register by successive sending on the data bus N passwords proper to the selected register during N first operations for selection of the register with $N \geq 1$, the selection of the register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

38. A method according to Claim 37, wherein the step of blocking comprises blocking selection of a selected register during read and write access operations to that register after each resetting of the microprocessor.

39. A method according to Claim 37, wherein the step of blocking comprises blocking selection of a selected register during write access operations to that register after each resetting of the microprocessor.

40. A method according to Claim 37, wherein each protection circuit is connected between an output of the address decoder and a selection input of an associated register for selection thereof.

41. A method according to Claim 37, wherein each protection circuit, during the N first operations for the selection of an associated register, compares N data elements present on the data bus with the N passwords proper to the associated register, and each protection circuit is released for subsequent operations of selection of the associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

42. A method according to Claim 37, wherein a single password is provided for each register; and wherein the steps of blocking and releasing comprises:

comparing, during a first operation for the selection of the register, a data element present on the data bus with the password proper to the register and for delivery of an output signal representing a result of the comparison;

holding in each protection circuit the output signal until the next resetting of the microprocessor; and

permitting the selection of the register for the subsequent selection operations of the register if the output signal indicates that the data present on the data bus during the first operation of selection of the register corresponds to the password associated with the register.